Analysis and Controller Design of Static Var Compensator Using Three-Level GTO Inverter

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Abstract—A static var compensator (SVC) using three-level GTO voltage source inverter (VSI) is presented for high-voltage, high-power applications. The three-level VSI has lower harmonic components and higher dc-link voltage than the two-level VSI and thus can be operated at lower switching frequency \( f_{sw} \leq 500 \text{ Hz} \) without excessive harmonic contents. From the DQ-transformed equivalent circuit of the presented SVC system, DC and AC analyses are carried out to know the steady state and the dynamic characteristics of the system. Based on the open-loop transfer function of the system, a controller is designed to achieve fast dynamic response. The experimental results confirm the theoretical analyses and controller design.

I. INTRODUCTION

It is well-known that there has been a large demand for high-power, high-voltage static var compensator (SVC) systems to regulate and stabilize transmission lines and to compensate industrial lagging loads. Various passive and active static var compensators have been reported in the literature.

In the earlier SVC's, multi-inverter systems for large-scale reactive power compensation are developed because of the lack of high-power, self-commutated semiconductor switches and the desire to reduce the harmonics. These inverters are made up of large problematics series/parallel connections with special transformer arrangements in order to reduce the harmonic contents caused by each inverter. Because of the number of inverter stages or harmonic filter legs, however, such an SVC system becomes expensive, complicated, and large in volume, and suffers from resonances created by peripheral harmonic current sources.

The possibility of pulse-width modulation (PWM) voltage source inverters with high switching frequency for reactive power compensation is also reported. However, the high switching frequency operation of presently available high-power semiconductor devices, like gate turn-off thyristors (GTO's), is not available. The switching frequency of GTO may not exceed several hundred hertz \( f_{sw} < 500 \text{ Hz} \), especially in the high-power range where high voltage can be applied. Recently, in order to apply to large-scale reactive power compensation, new SVC systems with low switching frequency PWM operation have been reported. However, heavy harmonic filter legs should be utilized to prevent the injection of excessive harmonic currents caused by low switching frequency PWM operation into the AC mains.

The aforementioned SVC's are made up of two-level voltage source inverters. A neutral-point-clamped inverter (NPC inverter, also called three-level inverter) is reported in the literature. The three-level inverter has the advantages that the blocking voltage of each switching device is one half of dc-link voltage whereas full dc-link voltage for two-level inverter, and the harmonic contents of three-level inverter output voltage are far less than those of two-level one at the same switching frequency. Thus three-level inverters can be operated at lower switching frequency \( f_{sw} < 500 \text{ Hz} \) without excessive harmonic currents and can be coupled directly to 3.3
kV ac mains using 4500 V GTO's. These advantages enable the SVC system using a three-level inverter to be suitable for large-scale reactive power compensation.

This paper presents the SVC system using a three-level GTO voltage source inverter for high-power, high-voltage applications. A new modeling method of the SVC system using a three-level inverter is reported by the authors [9]. A general and simple model for the proposed SVC system is derived by using the circuit DQ transformation [10]. First the DQ-transformed equivalent circuit for the proposed SVC system is obtained, and then it is analyzed completely, including dc and ac characteristics. In addition, the controller design based on the open-loop transfer function of the system obtained by the analysis of the DQ-transformed equivalent circuit is presented in this paper.

II. BRIEF SYSTEM OVERVIEW

The simplified block diagram of the SVC system presented in this paper is shown in Fig. 1. The SVC system consists of a three-level inverter, a set of linked reactors and series-connected dc capacitor tanks, the three-phase loads, and the ac mains.

Fig. 2(a) shows the structure of one pole of the three-level GTO inverter, and the associated switching table is shown.
in Fig. 2(b). The voltage stress of each switching device is clamped to one half of the dc-link voltage \(V_{dc}\), whereas full dc-link voltage \(2V_{dc}\) for two-level conventional inverter and thus power devices could be fully utilized in the high-voltage range. The inverter output voltage waveform \(v_s\) is made up of three-state voltages \(+V_{dc}, 0, -V_{dc}\) and thus shows relatively lower harmonic contents in the line currents and requires smaller filter size.

The operating principles of the SVC system can be explained by considering the per-phase fundamental equivalent circuit of the SVC systems. An equivalent voltage source \(V_{oal}\) is connected to the ac mains through a linked reactor \(L\) and a resistor \(R_s\) representing the total losses in the inductor, including the inverter, as shown in Fig. 3(a). By controlling the phase angle \(\alpha\) of the inverter output voltage with respect to the phase of source voltage, the dc capacitor voltage \(V_{dc}\) can be changed. Thus, the amplitude of the fundamental component of the inverter output voltage \(V_{oal}\) can be controlled. Fig. 3(b) and (c) shows the phasor diagram for leading (capacitive) and lagging (inductive) var generation, respectively.

A more detailed explanation is described in Section IV by analyzing the DQ-transformed equivalent circuit obtained in the next section.

### III. Modeling

The simplified main circuit of the SVC system is shown in Fig. 4. By using circuit DQ transformation method, modeling of this circuit is presented by the authors [9]; however, for convenience, the modeling of this circuit is reviewed here. Modeling is carried out under the following assumptions:

1. all switches are ideal,
2. the source voltages are balanced,
3. the total losses in the inverter are represented by lumped resistor \(R_s\), and
4. the harmonic contents caused by switching action are negligible.

The original circuit is too complex to analyze, so it is partitioned into several basic subcircuits, as shown in Fig. 4. The three-phase source voltage \(v_{s,abc}\) and DQ transformation matrix \(K\) are defined as follows:

\[
v_{s,abc} = \begin{bmatrix} v_{sa} \\
                          v_{sb} \\
                          v_{sc} \end{bmatrix} = \sqrt{2/3}V_s \begin{bmatrix} \sin(\omega t) \\
                          \sin(\omega t - 2\pi/3) \\
                          \sin(\omega t + 2\pi/3) \end{bmatrix}
\]

\[v_s = \frac{\sqrt{2}}{\sqrt{3}}V_s \begin{bmatrix} \sin(\omega t) \\
                          \sin(\omega t - 2\pi/3) \\
                          \sin(\omega t + 2\pi/3) \end{bmatrix} \]

\[K = \begin{bmatrix} \cos(\omega t + \alpha) & \cos(\omega t - 2\pi/3 + \alpha) & \cos(\omega t + 2\pi/3 + \alpha) \\
                        \sin(\omega t + \alpha) & \sin(\omega t - 2\pi/3 + \alpha) & \sin(\omega t + 2\pi/3 + \alpha) \end{bmatrix} \]

\[\frac{1}{\sqrt{2}} \quad \frac{1}{\sqrt{2}} \quad \frac{1}{\sqrt{2}} \]

where the \(V_s\) and \(\omega\) denote the rms line-to-line voltage and the angular frequency of the source voltage, respectively, and the variable \(\alpha\) is the phase angle of matrix \(K\).

A variable \(x_{abc}\) that denotes any ac voltages and currents is transformed into \(x_{qdo}\) by DQ transformation matrix \(K\):

\[x_{qdo} = Kx_{abc}, \quad x_{abc} = K^{-1}x_{qdo}.\]

### A. Transformation of Part A

The relationship between voltage and current in the resistor \(R_s\) gives

\[v_{s,abc} = R_s i_{abc} + v_{abc} \]

and the circuit DQ-transformed result of (5) is given by

\[v_{s,qdo} = R_s i_{qdo} + v_{qdo} \]

where

\[v_{s,qdo} = Kv_{s,abc} = V_s \begin{bmatrix} -\sin \alpha & \cos \alpha & 0 \end{bmatrix}^T.\]
Fig. 8. Plot of $Q_c$ and $P_c$ drawn by the inverter versus $\alpha$.

B. Transformation of Part B

The relationship between voltage and current in the inductor $L$ gives

$$L \frac{d}{dt} i_{abc} = v_{abc} - v_o,abc.$$  \hspace{1cm} (8)

and the circuit DQ-transformed result of (8) is given by

$$L \frac{d}{dt} i_{qdo} = L \frac{d}{dt} K^{-1} i_{qdo} + v_{qdo} - v_o,qdo.$$ \hspace{1cm} (9)

That is

$$L \frac{d}{dt} i_{q} = -\omega L i_d + v_q - v_oq,$$ \hspace{1cm} (10)

$$L \frac{d}{dt} i_d = \omega L i_q + v_d - v_{od}.$$ \hspace{1cm} (11)

From (10) and (11), the inductor set becomes a second order gyrator-coupled system, as shown in Fig. 5(b).

C. Transformation of Part C

Under the assumption that the harmonic components caused by switching action in the inverter are negligible, a switching function $S$ can be defined as follows:

$$S = \begin{bmatrix} S_o \\ S_B \\ S_c \end{bmatrix} = \sqrt{2/3}D \begin{bmatrix} \sin(\omega t + \alpha) \\ \sin(\omega t - 2\pi/3 + \alpha) \\ \sin(\omega t + 2\pi/3 + \alpha) \end{bmatrix}.$$ \hspace{1cm} (12)

The phase angle $\alpha$ is the phase difference between source voltage given by (1) and the switching function given by (12) and is equal to the phase angle of the transformation matrix $K$. Using the switching function $S$, the part C is expressed as follows:

$$v_o,abc = S v_{dc},$$ \hspace{1cm} (13)

$$i_{dc} = \frac{1}{2} S^T i_{abc},$$ \hspace{1cm} (14)

$$i_{dc} = C \frac{di_{dc}}{dt}.$$ \hspace{1cm} (15)

Note that from (13) the amplitude, $\sqrt{2/3}D$, in (12) indicates the modulation index (MI) of the switching function $S$. Applying the matrix $K$ to (13) and (14) yields the following equations:

$$v_o,qdo = K v_{o,abc} = \begin{bmatrix} 0 & D & 0 \end{bmatrix}^T v_{dc},$$ \hspace{1cm} (16)

$$i_{dc} = \frac{1}{2} S^T K^{-1} i_{qdo}.$$ \hspace{1cm} (17)

From (15)–(17), the part C becomes a transformer-coupled system, as shown in Fig. 5(c). It is worthy to note that there is no difference in modeling between two-level and three-level inverters because the fundamental component is only considered under the assumption that harmonic components are negligible. That is, if the modulation indexes of PWM patterns are the same, the transformed equivalent circuits are identical.
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Meaning of fundamental frequency and fundamental angular frequency.

\[
\text{rms line-to-line voltage} = V_s = 550 \text{ [V]}
\]
\[
\text{effective resistance} = R_s = 0.4 \text{ [Ω]}
\]
\[
\text{linked reactor} = L = 10 \text{ [mH]}
\]
\[
\text{DC-side capacitor} = C = 1000 \text{ [μF]}
\]

D. Circuit Reconstruction

The rule of circuit reconstruction is to connect the adjacent related nodes where the voltage and current variables are the same. The result is shown in Fig. 6. This circuit can be directly used to find the dc operating point and dynamics of the system.

IV. ANALYSES

From the equivalent circuit obtained in the previous section, dc analysis is done to know the steady state operation and ac analysis is achieved to find the transient characteristics of the system.

A. DC Analysis

In the steady state operation, the inductors seem to be short and the capacitor seems to be open since all the DQ circuit variables imply dc values denoted by capital letters. Thus, using the equivalent circuit for dc, as shown in Fig. 7, the characteristics of the SVC system in the steady state can be obtained without cumbersome equational manipulations. From Fig. 7, we obtain

\[
V_{sq} = -V_s \sin \alpha,
\]
\[
V_{sd} = V_s \cos \alpha,
\]
\[
I_q = -\frac{V_s}{R_s} \sin \alpha,
\]
\[
I_d = 0,
\]
\[
V_{dc} = \frac{V_s}{D} \left( \cos \alpha - \frac{\omega L}{R_s} \sin \alpha \right).
\]

Therefore, the real power \( P_c \) and the reactive power \( Q_c \) drawn by the inverter system are expressed as

\[
P_c = V_{sq} I_q + V_{sd} I_d = \frac{V_s^2}{2R_s} \left( 1 - \cos(2\alpha) \right)
\]
\[
Q_c = V_{sq} I_d - V_{sd} I_q = \frac{V_s^2}{2R_s} \sin(2\alpha).
\]

Fig. 8 shows the magnitude of \( P_c \) and \( Q_c \) as a function of \( \alpha \) with the specific circuit parameters given in Table I. The real power \( P_c \) corresponds to the total losses in the inverter. Note that in the range of small \( \alpha \), i.e., \( |\alpha| < 5^\circ \), the amount of reactive power is almost proportional to \( \alpha \). It can be seen that \( Q_c \) is dependent on only control variable \( \alpha \) not on the circuit parameters, i.e., \( L \) and \( C \). In addition, \( V_{dc} \) is dependent on the \( \alpha \), MI of switching pattern and the value of \( L \) but independent of the value of \( C \).
Fig. 12. Unit step response of the closed-loop SVC system, $\dot{Q}_c(s)/\dot{Q}_c^*(s)$ for $\alpha \approx 0$.

Fig. 13. The optimized three-level switching pattern for three-level inverter.

B. AC Analysis

The ac analysis can be done by introducing some perturbations in the control variable $\alpha$. At this point, the circuit variables consist of dc and ac components and thus the perturbed components (ac values) are indicated by diacritical mark $\dot{}$ of the corresponding variables to distinguish from the quiescent values. Also, the following assumptions are made:

1) the quiescent $\alpha$ is nearly zero,
2) the perturbed $\dot{\alpha}$ is small ($|\dot{\alpha}| < 5^\circ$), and
3) the second-order terms, i.e., products of variations, are negligible. With the aforementioned assumptions, we obtain

$$\dot{v}_{sd} = V_e \sin(\alpha + \dot{\alpha}) + V_e \sin \alpha \approx -V_e \dot{\alpha} \tag{23}$$

Therefore, the resultant small signal equivalent circuit can be drawn as shown in Fig. 9, where all the dc components are eliminated. Now, it is straightforward to get the state equation of the system. The input of the system is the control variable $\alpha$ and the output is the generated reactive power $Q_c$. From Fig. 9, we have

$$\frac{dx}{dt} = A x + B \dot{\alpha} \tag{26}$$

$$\dot{Q}_c = C x \tag{27}$$

where

$$x = [\dot{i}_d \dot{i}_d \dot{v}_{dc}]^T \tag{28}$$

$$A = \begin{bmatrix} -R_e/L & -\omega & 0 \\ \omega & -R_e/L & -D/L \\ 0 & D/2C & 0 \end{bmatrix} \quad B = \begin{bmatrix} -V_e/L \\ 0 \end{bmatrix} \tag{29}$$

$$C = [-V_e \ 0 \ 0]. \tag{30}$$
From (26) and (27), the transfer function of the system is given by
\[
\frac{\dot{Q}_c(s)}{a(s)} = C(sI - A)^{-1}B = \frac{N(s)}{M(s)}
\] (31)

where
\[
N(s) = \frac{V_s^2}{L} \left[ s^2 + \frac{R_s}{L} s + \frac{D^2}{2LC} \right]
\] (32)
\[
M(s) = s^3 + \frac{2R_s}{L} s^2 + \left( \frac{R_s}{L} \right)^2 \left( \frac{D^2}{2LC} + \omega^2 \right) s + \frac{D^2 R_s}{2L^2 C}
\] (33)

Fig. 10 shows the unit step response of the open-loop system with the circuit parameters given in Table I. It can be seen that the SVC system takes about 15 cycles, 250 ms, to reach another steady state.

V. CONTROLLER DESIGN

From the transfer function of (31), a controller can be designed in order that the var compensator system has fast dynamic characteristics. Fig. 11 shows the block diagram of the closed-loop system constructed by PI controller. The open-loop system transfer function \(G_p(s)\) is given by (31), and the transfer function of the controller is expressed as
\[
G_c(s) = K_p + \frac{K_i}{s}
\] (34)
The closed-loop transfer function is given by

\[
\frac{\hat{Q}_c(s)}{\hat{Q}_s^*(s)} = \frac{G_c(s)G_p(s)}{1 + G_c(s)G_p(s)}.
\]

To achieve fast dynamic response of the closed-loop system with the circuit parameters given in Table I, the control parameters are determined as follows:

\[K_p = 1 \times 10^{-5}, \quad K_i = 1.7 \times 10^{-4}.\]  (36)

Fig. 12 shows the unit step response of the closed-loop system for the designed control parameters in (36) with the circuit parameters given in Table I. The SVC system takes two cycles to reach another steady state.

VI. EXPERIMENTAL RESULTS

To confirm the validity of the proposed analysis and controller design, an experimental 30 kVA prototype is implemented and tested. A three-phase, three-level GTO inverter is constructed with the values given in Table I. An optimized three-level PWM waveform is employed so as to meet the switching characteristics of the GTO device. Supposing high-power operation, the switching frequency at each active device is chosen to be relatively low. Fig. 13 shows the three-level switching pattern with respect to the phase voltage of the ac mains where the switching frequency of each device is considered to be 180 Hz. The PWM switching angles used in the experiment are

\[\beta_1 = 10^\circ, \quad \beta_2 = 16^\circ, \quad \beta_3 = 22^\circ.\]  (37)

Fig. 14 shows the closed-loop system block diagram for implementation with PI controller. The control parameters, \(K_p\) and \(K_i\), are the same values designed in the previous section. In this experiment, the reactive load is not connected to the ac mains and the var command of the ac mains, \(Q^*_s\), is given arbitrary.

VII. CONCLUSION

In this paper, a SVC system using three-level GTO voltage source inverter is presented suitable for high-power, high-voltage applications. The general and simple DQ-transformed equivalent circuit for the proposed SVC system is obtained and analyzed completely, including dc and ac characteristics. In addition, based on the open-loop transfer function of the system obtained from the analysis of the DQ-transformed equivalent circuit, the PI controller is designed in order that the SVC system has fast dynamic response. The optimized

Fig. 15 shows the steady state results for the capacitive var generation; the var command of the ac mains, \(Q^*_s\), is ‘-30 kVAR’. Fig. 16 shows the steady state results for the inductive var generation. Figs. 15(a) and 16(a) show the ac line-to-line voltage \(v_{ma}\) and the inverter output line-to-line voltage \(v_{in}\). The phase angle ‘\(\alpha\)’ of the inverter output voltage is negative for capacitive var generation, as shown in Fig. 15(a), and positive for inductive var generation, as shown in Fig. 16(a). Figs. 15(b) and 16(b) show the ac line current \(i_a\) and the phase voltage \(v_{ma}\). Note that the line currents generated by the three-level inverter have low harmonic components even though the switching frequency of the active devices is 180 Hz.

Figs. 17 and 18 show the transient responses of the SVC system for a step change in the var command from capacitive to inductive and vice versa. Note that the unit step response of the open-loop system is very slow (about 15 cycles, 250 ms), as shown in Fig. 10. These figures show that the SVC system takes about three cycles to reach another steady state. For the reason of the approximation in the analysis and the low-pass filter used to filter the reactive power \(Q_s\) in the experiment, the experimental step response is thought to be slowed down one cycle more, compared with the analytical step response. The experimental results are thought to confirm the theoretical analysis and controller design pretty closely.
PWM pattern with low switching frequency \( f_{sw} = 180 \text{ Hz} \) is adopted to be suitable for large reactive power compensation.

The validity of the analysis and controller design is proved by the experimental results. The line currents generated by the three-level inverter have low harmonic components even though the switching frequency of the active devices is very low. Good overall performance is obtained.

REFERENCES


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